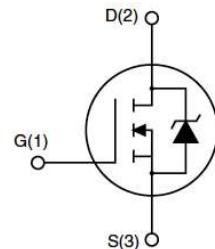


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N-Channel Power MOSFET

Features

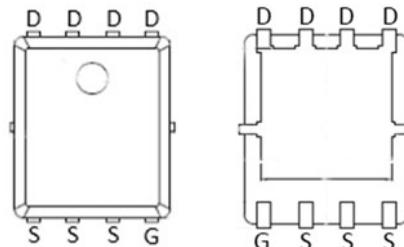
- 30V,180A
- $R_{DS(ON)} = 1.7 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10\text{V}$
- $R_{DS(ON)} = 3.2 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 4.5\text{V}$
- Low Total Gate Charge
- Low Reverse Transfer Capacitance
- Improved dv/dt Capability
- Fast Switching Speed



Application

- Load Switch
- PWM Application

Package



PDFN5X6

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
180N03G	AP180N03G	PDFN5X6	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a = 25^\circ\text{C}$)	I_D	180	A
Continuous Drain Current ($T_a = 100^\circ\text{C}$)	I_D	115	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	720	A
Singel Pulsed Avalanche Energy ⁽²⁾	E_{AS}	306	mJ
Power Dissipation	P_D	130	W
Thermal Resistance,Junction to Case ⁽⁴⁾	R_{eJC}	0.97	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS} = 30V, V_{GS} = 0V, T_J = 55^\circ\text{C}$	--	--	5	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.7	2.4	V
Drain-Source On-Resistance (Note3)	$R_{DS(\text{on})}$	$V_{GS} = 10V, I_D = 30\text{A}$	--	1.7	2.1	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 20\text{A}$	--	3.2	4.0	$\text{m}\Omega$
Forward Transconductance (Note3)	g_{fs}	$V_{DS} = 10V, I_D = 20\text{A}$	20.8	--	--	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 15V,$ $f = 1.0\text{MHz}$	--	4300	--	pF
Output Capacitance	C_{oss}		--	720	--	
Reverse Transfer Capacitance	C_{rss}		--	420	--	
Total Gate Charge	Q_g	$V_{DD} = 15V, I_D = 20\text{A},$ $V_{GS} = 10V$	--	70	--	nC
Gate-Source Charge	Q_{gs}		--	10	--	
Gate-Drain Charge	Q_{gd}		--	15	--	
Turn-on Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15V, R_G = 3\Omega$	--	10	--	ns
Turn-on Rise Time	t_r		--	6.5	--	
Turn-off Delay Time	$t_{d(\text{off})}$		--	75	--	
Turn-off Fall Time	t_f		--	18	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_s	$T_C = 25^\circ\text{C}$	--	--	150	A
Pulsed Diode Forward Current	I_{SM}		--	--	720	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 30\text{A}, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 20\text{A},$ $di_F/dt = 100\text{A}/\mu\text{s}$	--	30	--	ns
Reverse Recovery Charge	Q_{rr}		--	15	--	nC

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J=25^\circ\text{C}, V_{DD}=15V, R_G=25\Omega, L=0.5\text{mH}$
3. Pulse Test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10$ sec

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Typical Performance Characteristics

Figure 1: Output Characteristics

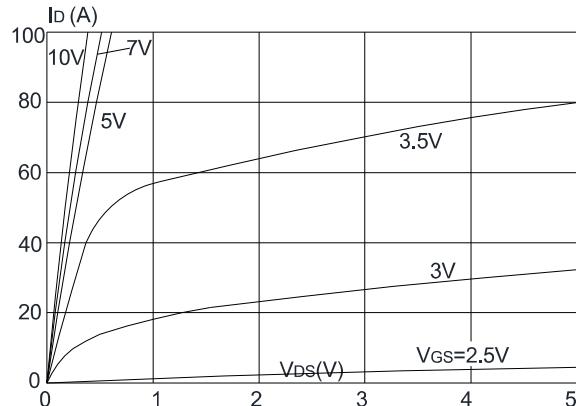


Figure 2: Typical Transfer Characteristics

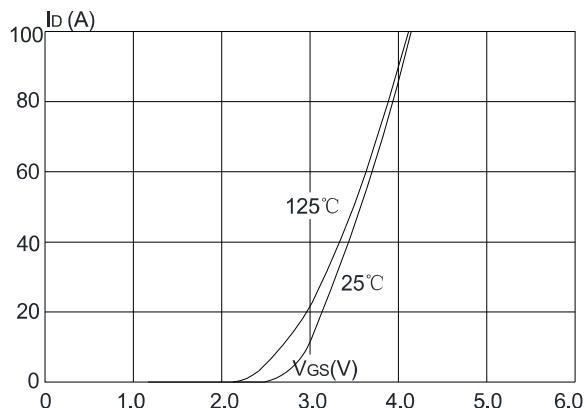


Figure 3: On-resistance vs. Drain Current

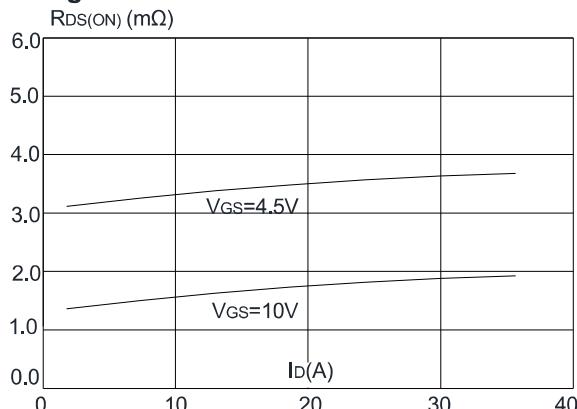


Figure 5: Gate Charge Characteristics

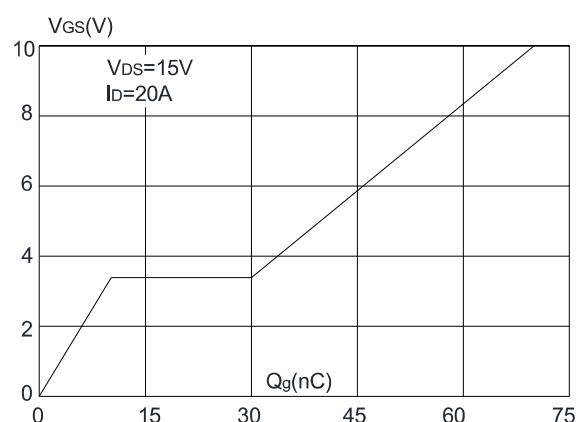


Figure 4: Body Diode Characteristics

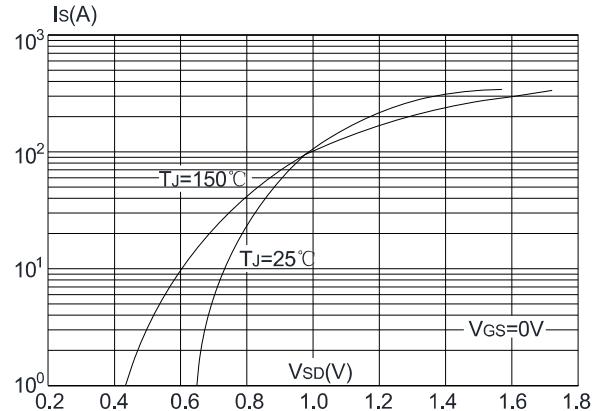
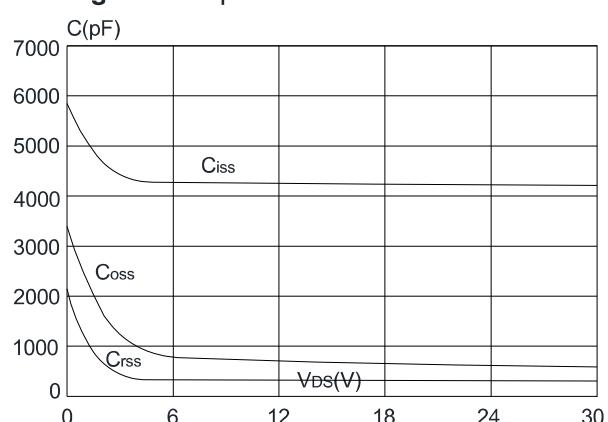


Figure 6: Capacitance Characteristics



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Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

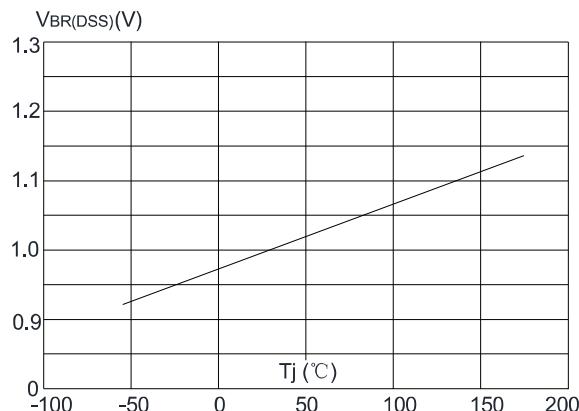


Figure 8: Normalized on Resistance vs. Junction Temperature

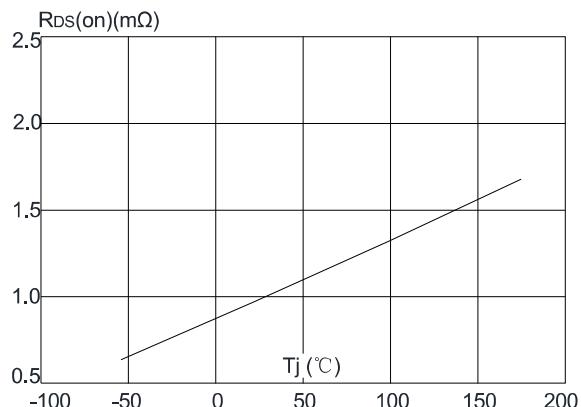


Figure 9: Maximum Safe Operating Area

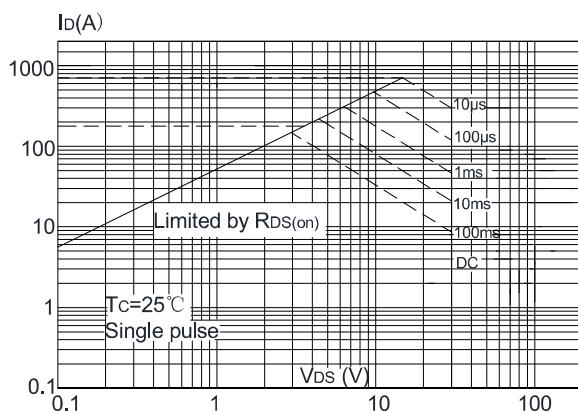


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

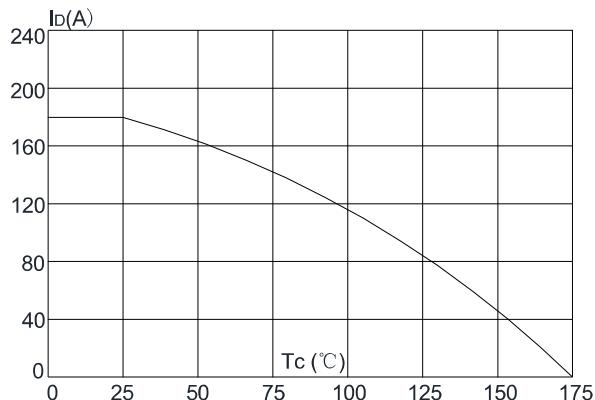
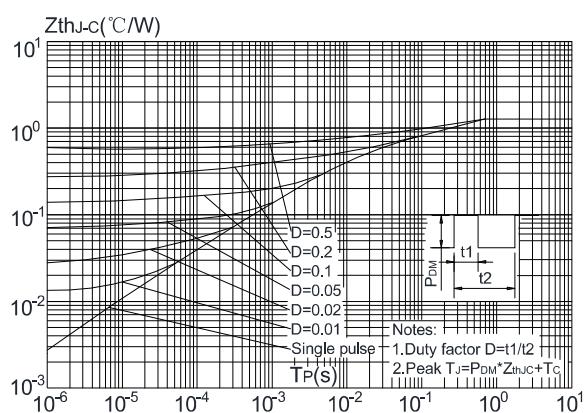


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



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Figure 1 : Gate Charge Test Circuit and Waveform

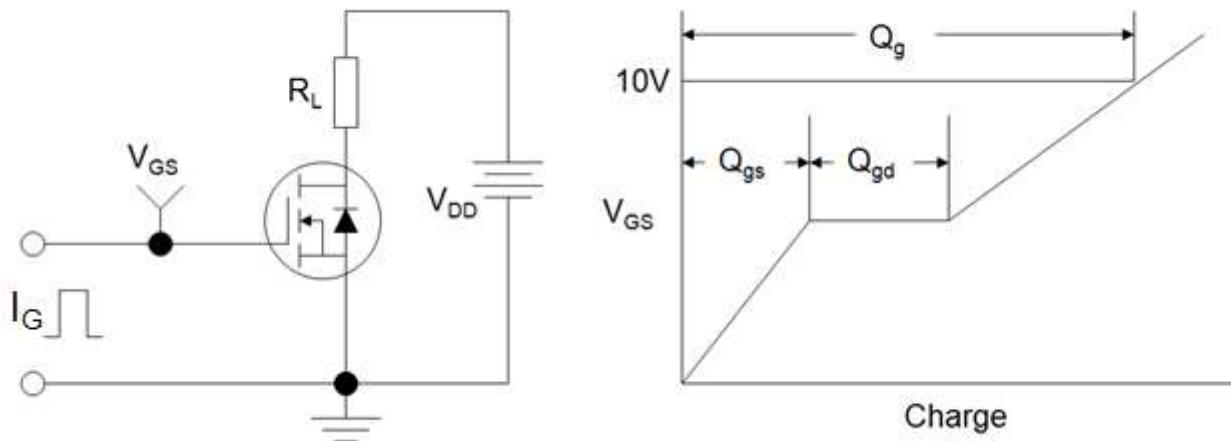


Figure 2 : Resistive Switching Test Circuit and Waveform

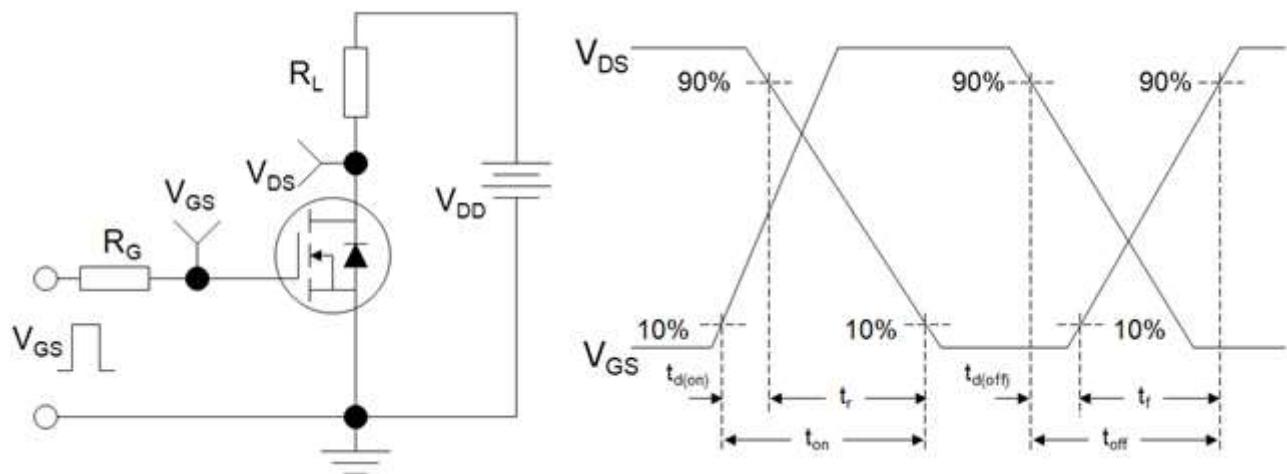
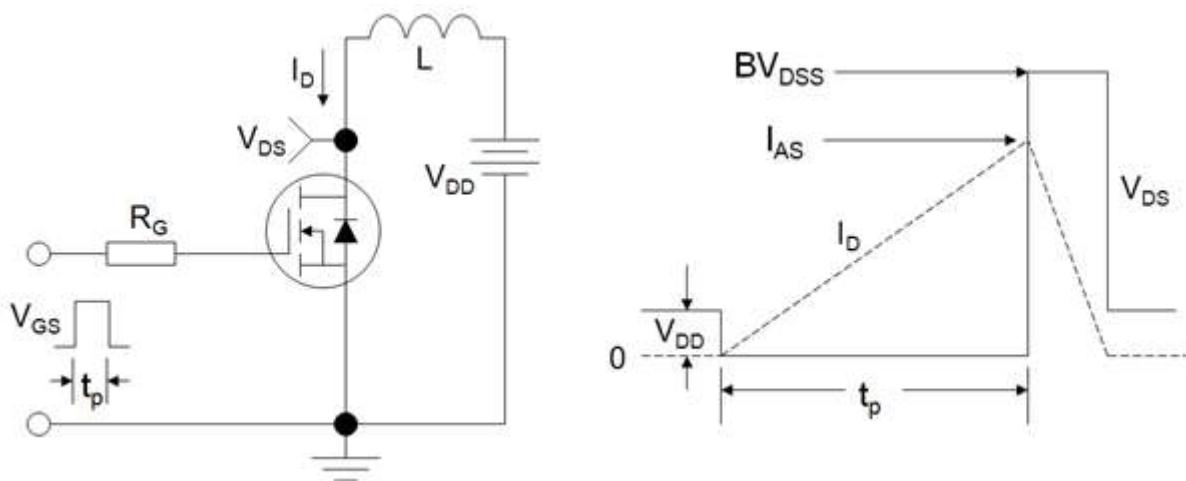
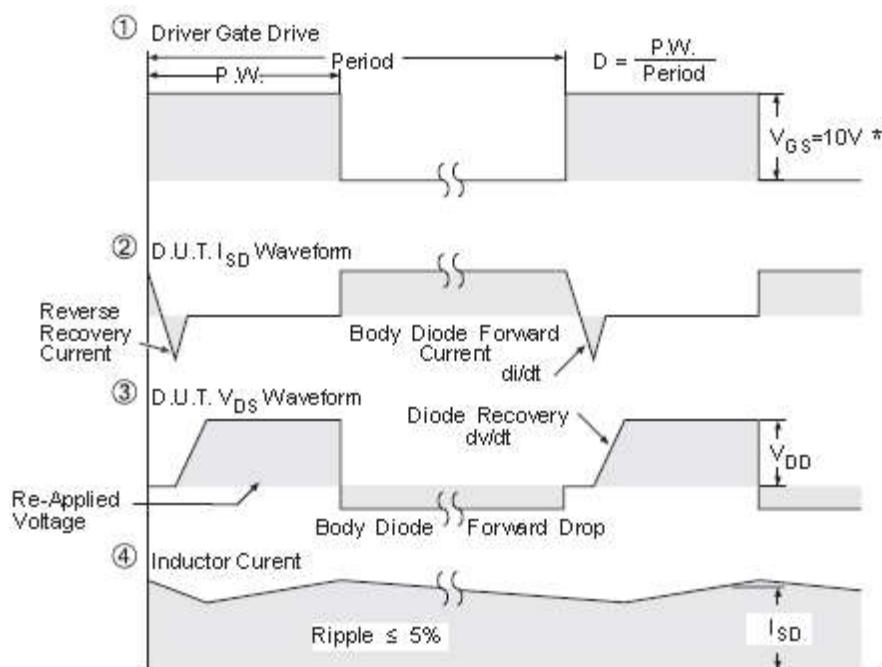
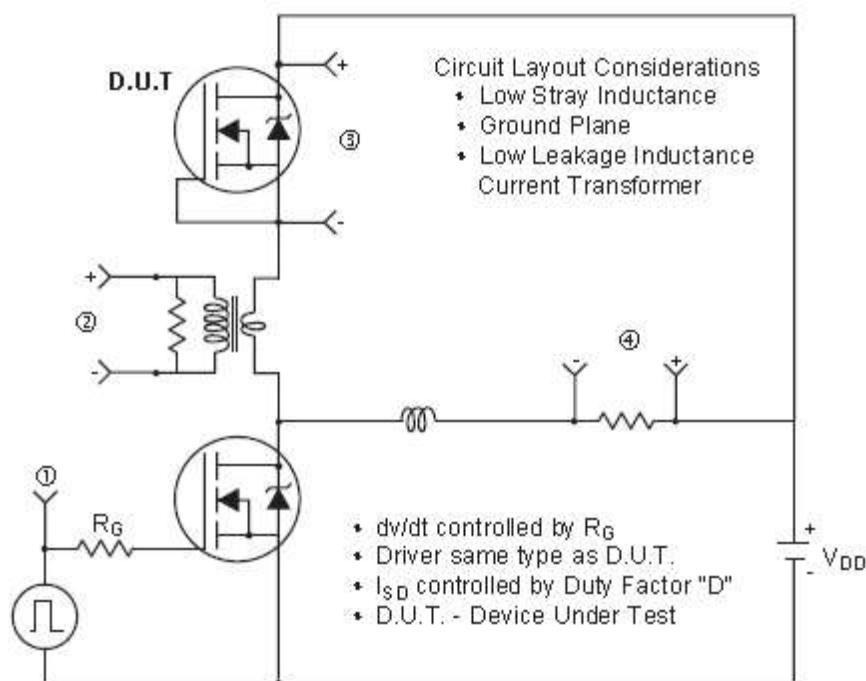


Figure 3 : Unclamped Inductive Switching Test Circuit and Waveform



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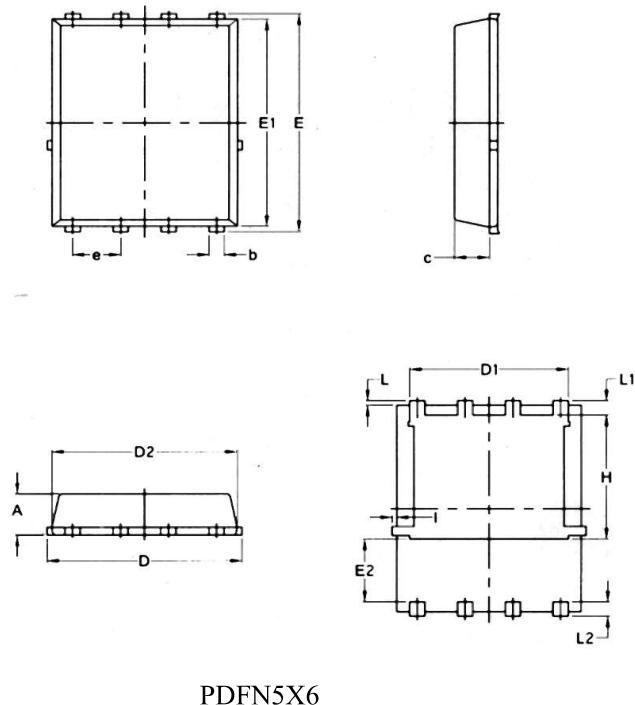
* $V_{GS} = 5V$ for Logic Level Devices

Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

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Package Mechanical Data



PDFN5X6

SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	—	0.0630	—
e	1.27	BSC	0.05	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070

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